

## Jz4740 Version-Mark vs Function

### Revision History

Revision	Date	Author	Description
1.0	07-Jul-26	Zhang Jin	Original

### 1. Version & Mark

Version	Mark	Description
MPW	070307S0316A	
A0	070618S0621A	
A1	0708??S08??A	The mark is to be decided
B	07????S????A	The mark is to be decided

### 2. Functions changed from version MPW to Version A0

- a) **SSI**: Extend TFIFO and RFIFO from 16-level to 128-level, then update **SSICR1.TTRG** & **SSICR1.RTRG** from 2 bit to 4 bit, **SSISR.RFIFO\_NUM** & **SSISR.TFIFO\_NUM** from 5 bit to 8 bit.
- b) **EMC**: remove ECC bug
- c) **USB Device 2.0 PHY**: RREF should be connected to a 2.5k resistor and VDDA with a 1uf and a 0.1uf capacitors. Furthermore, PHY's EOP timing was update so that it can run normally when it is inserted into jz4740 host.
- d) **UART**: One UART port (UART1) added. UART1\_RxD is multiplexed with UART0\_CTS\_; UART1\_TxD is multiplexed with UART0\_RTS\_.
- e) **DMAC**: remove a bug and add DMA for UART1
- f) **CPM**: In spec, add clock divider register (**SSICDR**) for fast SSI clock, you may select 12M or fast SSI clock with **SSICDR.SCS** bit. Add uart1 clock gate in **CLKGR** register.
- g) **SADC**:  
In spec, Bit31: 30 are added and bit14: 13 are changed in Register **ADCFG**.

Bit31: The XdYdZmZn of the same point measure can be set to same or different.

Bit30, bit14 and bit13: Choose external driver or internal driver when sample.

- h) **GPIO**: Interrupt flag is cleared by writing 1 to PDATC in MPW, to PDATS/PFLAGC now. UART1 GPIO added. Level interrupt can't be saved in register in now but can be saved in MPW.
- i) **LCDC**: Bit7 is added and bit3:0 is changed in register **LCDCFG**. Bit7 is used to choose 16-bit parallel TFT LCD and 18-bit parallel TFT. Bit3:0-bit to choose the special or normal TFT for 16/18-bit parallel TFT.

LCD and SLCD Pin configure is changed as the following:

Old Pin configure:

LCDPIN	PIN25	PIN24	PIN23	PIN22	PIN21	PIN20	PIN19	PIN18	PIN17-0
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0	LCD PCLK	LCD VSYNC	LCD HSYNC	LCD DE	LCD REV	LCD PS	LCD CLS	LCD SPL	LCD D [17:0]
1				SLCD CS	SLCD CLK	SLCD RS			SLCD D [17:0]

New Pin configure:

LCDPIN	PIN25	PIN24	PIN23	PIN22	PIN21	PIN20	PIN19	PIN18	PIN17-0
0	LCD PCLK	LCD VSYNC	LCD HSYNC	LCD DE	LCD REV	LCD PS	LCD CLS	LCD SPL	LCD D [17:0]
1	SLCD CLK	SLCD CS	SLCD RS						SLCD D [17:0]

- j) **SLCD**: Bug removed . Old design will lose command/data when the freq of clock is to fast. New design will not lose command/data when the freq of clock is to fast.
- k) TCU: spec not changed.
- l) **AIC/CODEC**: Register: CDCCR1.SW2ON was reset to 1, is reset to 0.
- m) **RTC-HIB**:
  - HWCR register is changed, remains only one bit field: EALM. All other fields are removed
  - A power-off detection circuit is added. When VDDHP is found power down, the chip enters hibernating mode automatically
  - RTCCR.AE was not changed during reset, is reset to 0 by PPRST\_ and HRST\_
  - RTCCR.RTCE was reset by PPRST\_ only, is reset by both of PPRST\_ and HRST\_
  - WKUP\_ pin wakeup was valid in either high or low decided by register setting, is valid only in low
  - PWRON\_ was normal output pin, is open-drain output pin
  - PPRST\_ and WKUP\_ were normal input pins, are Schmitt trigged input pins
  - VDDRTC is changed from 3.3V to 1.8V. The high voltage of input signal PPRST\_ and WKUP\_ is changed as well (from 3.3V to 1.8V)

### 3. Functions changed from version A0 to Version A1

- a) In A0 version, pins of GPD26, GPD27, GPD28 and GPD30 are output 0 during reset (PPRST\_, Hibernating-reset and WDT-reset). In A1 version, these pins are input pull-up during reset
- b) In A0 version, PBAT input signal voltage cannot be > VDDADC + 0.3V. In A1 version, PBAT signal voltage can be 5V.

### 4. Functions changed from version A1 to Version B

- a) VDDRTC is changed from 1.8V to 3.3V. The high voltage of input signal PPRST\_ and WKUP\_ is changed as well (from 1.8V to 3.3V)